

ABSTRACT

The present invention relates to a decoding apparatus and a decoding method for realizing the decoding of LDPC codes, in which, while the circuit scale is suppressed, the 5 operating frequency can be suppressed within a sufficiently feasible range, and control of memory access can be performed easily, and to a program therefor. A check matrix of LDPC codes is formed by a combination of a  $(P \times P)$  unit matrix, a matrix in which one to several 1s of the unit 10 matrix are substituted with 0, a matrix in which they are cyclically shifted, a matrix, which is the sum of two or more of them, and a  $(P \times P)$  0-matrix. A check node calculator 313 simultaneously performs p check node calculations. A variable node calculator 319 simultaneously 15 performs p variable node calculations.